Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) Nonvolatile semiconductor memory cell having a substrate (1), which has a source region (7), a drain region (8) and a channel region lying in between, a first insulation layer (2), an electrically non conductive charge storage layer (3), a second insulation layer (4) and an electrically conductive control layer (10) being formed essentially at the surface of the channel region, and

the electrically non-conductive charge storage layer (3) having an interruption (U) in order to form a first and a second memory location (LB, RB),

characterized in that

the first and second memory locations (LB, RB) are locally delimited.

2. (Original) Nonvolatile semiconductor memory cell according to Patent Claim 1,

characterized in that the first and/or second insulation layer (2, 4) likewise has an interruption (U).

3. (Currently amended) Nonvolatile semiconductor memory cell according to ~~Patent~~ Claim 1 ~~or 2~~,

characterized in that the interruption (U) is at least partly filled with a third insulation layer (9).

4. (Original) Nonvolatile semiconductor memory cell according to Patent Claim 3,

characterized in that the electrically conductive control layer (10) is formed in the at least partly filled interruption (U).

5. (Currently amended) Method for fabricating a nonvolatile semiconductor memory cell, ~~having~~ the method comprising the following steps:

a) formation of a first insulation layer (2), an electrically non-conductive charge storage layer (2), a second insulation layer (4) and a mask layer (5) on a substrate (1);

b) patterning of the mask layer (5);

c) formation of sidewall layers (6) at the patterned mask layer (5);

d) removal of at least the second insulation layer (4) and the charge storage layer (3) using the patterned mask layer (5) and the sidewall layer (6);

e) formation of source and drain regions (7, 8) in the substrate (1);

f) removal of the mask layer (5);

g) removal of the second insulation layer (4), the charge storage layer (3) and the first insulation layer (2) using the sidewall layers (6);

h) removal of the sidewall layers (6); i) formation of a third insulation layer (9);

j) formation of an electrically conductive control layer (10);

k) patterning of the control layer (10) in order to form word lines (WL); and

l) removal of the third insulation layer (9), the second insulation layer (4), the charge storage layer (3) and the first insulation layer (2) using the patterned control layer (10) in order to form locally delimited memory locations (LB, RB).

6. (Original) The method as claimed in Patent Claim 5, characterized by the following step

m) formation of a fourth insulation layer (11).

7. (Currently amended) Method according to ~~either of~~ Patent Claim ~~Claims~~ 5 ~~and 6~~,

characterized in that an anisotropic etching is carried out in step d), f), g) and/or l).

8. (Currently amended) Method according to ~~one of~~ Patent ~~Claims~~ Claim 5 ~~to 7~~, characterized in that a wet etching is carried out in step h).

9. (Currently amended) Method according to ~~one of~~ Patent ~~Claims~~ Claim 5 ~~to 8~~, characterized in that, in step e), an ion implantation using the first insulation layer (2) as screen material is used and the first insulation layer (2) is 5 subsequently removed (10).

10. (Currently amended) Method according to ~~one of~~ Patent ~~Claims~~ Claim 5 ~~to~~ 8, characterized in that

in step d), the first insulation layer (2) is furthermore removed; and in step e), an ion implantation is carried out directly into the substrate (1).

11. (Currently amended) ~~Device or method~~ Method according to ~~one of~~ Patent ~~Claims 1 to 10~~ Claim 5,

characterized in that a thickness of the first insulation layer (2) is greater than a material thickness for direct tunnelling.

12. (Currently amended) ~~Device or method~~ Method according to ~~one of~~ Patent ~~Claims 1 to 11~~ Claim 5,

characterized in that the first, second, third and/or fourth insulation layer (2, 4, 9, 11) [[has]] comprises SiO_2.

13. (Currently amended) ~~Device or method~~ Method according to ~~one of~~ Patent ~~Claims 1 to 12~~ Claim 5,

characterized in that the electrically non-conductive charge storage layer (3) [[has]] comprises Si_xO_y or Si_3N_4.

14. (Currently amended) ~~Device or method~~ Method according to ~~one of~~ Patent ~~Claims 1 to 13~~ Claim 5,

characterized in that the control layer (10) and/or the mask layer (5) [[has]] comprises doped polysilicon, a metal and/or siliconized semiconductor material.

15. (Currently amended) ~~Device or method~~ Method according to ~~one of~~ Patent ~~Claims 1 to 14~~ Claim 5,

characterized in that the substrate (1) [[has]] comprises Si.

16. (New) Nonvolatile semiconductor memory cell according to Patent Claim 1. characterized in that a thickness of the first insulation layer (2) is greater than a material thickness for direct tunnelling.

17. (New) Nonvolatile semiconductor memory cell according to Patent Claim 1, characterized in that the first, second, third and/or fourth insulation layer (2, 4, 9, 11) comprises SiO_2.

18. (New) Nonvolatile semiconductor memory cell according to Patent Claim 1, characterized in that the electrically non-conductive charge storage layer (3) comprises Si_xO_y or Si_3N_4.

19. (New) Nonvolatile semiconductor memory cell according to Patent Claim 1, characterized in that the control layer (10) and/or the mask layer (5) comprises doped polysilicon, a metal and/or siliconized semiconductor material.

20. (New) Nonvolatile semiconductor memory cell according to Patent Claim 1, characterized in that the substrate (1) comprises Si.